Semi Conductor

Energy bond in solid:

In an isolated atom the energy of electron in different orbit is called energy level. If there are two close atoms then the electron of one atom interacts with the electron of another atom. The position of electron changes. Each energy is splitted up into two energy level. If there are n atoms closely packed together as in the case of solid, then each energy level is splitted up into n-energy level. Thus a single energy level have a range of energy level called energy band. For energy level there is n-energy band. There are three types of energy band in solid:

1) Valence band: The electrons in the outermost orbit of an atom are called valence electrons. The energy band occupied by valence electrons is known as valence band. This energy band may be completely filled with electrons or partially but can never be empty

2) Conduction band: The energy band which lies above the valence band is known as conduction band. The electrons in conduction band are called conduction electrons. As the electrons get sufficient energy, they get transmitted to higher unfullfilled energy band which is known as conduction band. It may be either be filled partially or completely empty (in insulators).

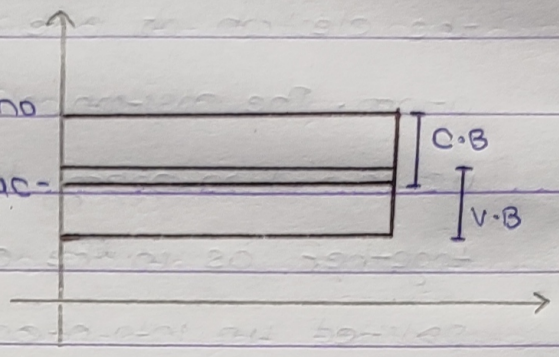
3) Forbidden energy gap: The separation between any two consecutive energy band is called forbidden energy gap. There is no electrons in this energy gap. The width of this gap between conduction band and valence band is different for different solids.

Classification of Solid: (on the basis of band theory)

Solids are divided into the following three class on the basis of energy band.

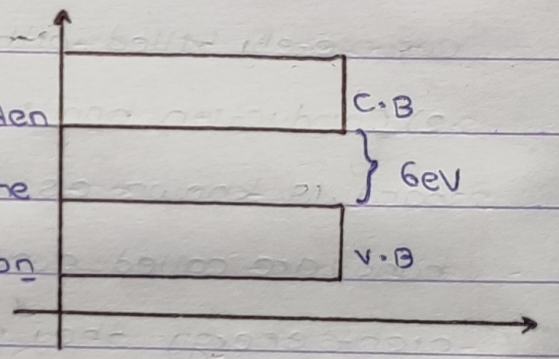
i) Conductor:

→ The materials in which there is no forbidden energy gap betwn conduction and valence band i.e. there occurs overlapping of these two bands. Due to overlapping betwn the V.B and C.B, the electrons of V.B are already present in the C.B. Thus, due to application of a very small p.d betwn the conductors the current flows through them easily. They have positive tempr coefficient of resistance so, its resistance increases with the rise in tempr and vice-versa.



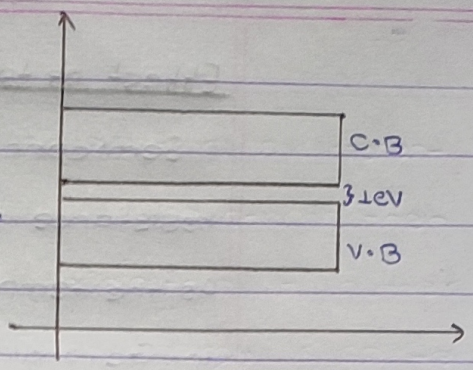
ii) Insulator:

→ The materials having large forbidden energy gap are called insulators. The energy gap is of about 6eV betwn V.B and C.B but can be more than this for some solids. As there is large energy gap, a very high electric field is required for the current to flow through them if possible. They have negative tempr coefficient of resistance so, resistance decreases with rise in tempr and vice-versa.

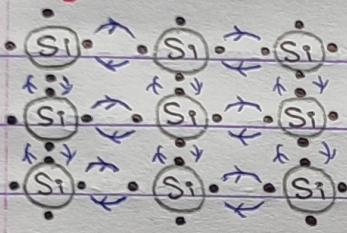


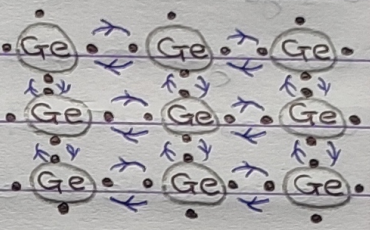
(ii) Semi-conductor:

→ The materials having forbidden energy gap of about 1eV are called semi-conductors. i.e. they have small energy gap betwn C.B & V.B. As there is small energy gap betwn C.B & V.B comparatively small electric field is required for causing the electrons to move from V.B to C.B. They behave as perfect insulator at about 0K. However, they conduct electricity at about room tempr as they have negative coefficient of resistance. Eg - Germanium (Ge) and silicon (Si).



Crystal Structure of Ge and Si:





Ge and Si atoms have four valence electrons in their outermost orbit. The four valence electrons of a particular Ge atom are shared with the four valence electron of the neighbouring 4 other atoms of the crystal to form covalent bond. This type of covalent bond is formed due to SP_3 hybridization and forms tetrahedral structure which is continued throughout the crystal. As all the valence electrons are used up for bond formation, there are no free electrons and do not conduct electric current at low tempr or 0K. They behave as an insulator at low tempr.

Effect of temperature or heating:

Semiconductor has negative temp^{r} coefficient of resistance so its resistance decreases with rise in temp^{r}. As the temperature increases, some of the covalent bond in Ge and Si crystal breaks. Due to breaking of bond free electrons are liberated which get transisted to the conduction band and hence electrical conductivity of crystals increases. As the electron get transisted it leaves a vacancy in its previous place i.e. valence band. This vacancy of electron in tetrahedral covalent structure is called positive hole as it behaves as positive charge. The hole are occupied by the electron of neighbouring atom and the new hole is created at that atom and so on. Thus, the effect is, motion of hole is in the opposite direction to the motion of electron inside the crystal. Thus, there are two current carriers i.e. free electrons and holes inside the crystal. So, Ge and Si crystal conducts electricity due to motion of holes and free electrons at high temp^{r} or even at room temp^{r}.

Types of semi-conductor:

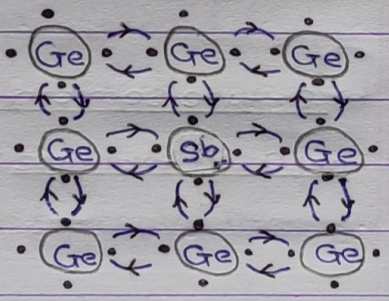
On the basis of purity of semiconductor they are of two types:

i) **Intrinsic or pure semi conductor:** A semiconductor in an extremely pure form is known as intrinsic semiconductor. No any types of impurities are dopped in the pure semiconductor. Thermally generated free electrons and hole are responsible for electrical conductivity. At about 0 kelvin, they behave as insulator but as the temp^r increases or even at room temp^r they conduct electricity slightly.

ii) **Extrinsic or impure semiconductor:** When either pentavalent or trivalent atoms or impurities are dopped to the lattice site of pure semiconductor, extrinsic semiconductor is formed. The process of adding impurities to the lattice site of pure semiconductor is known as dopping. The purpose of dopping is to increase the number of either free electrons or holes in semiconductor crystal which increases electrical conductivity.

On the basis of dopped atom, extrinsic semiconductors are of two types:

a) **N-type semi conductor or donor type:**

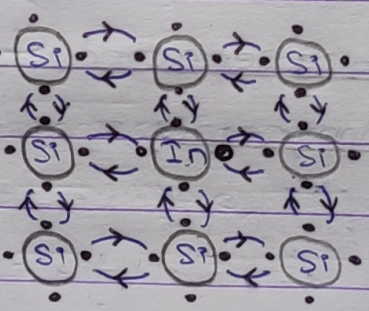


When pentavalent impurity or atoms like antimony (Sb) are dopped to pure Ge or Si crystal, then the resulting crystal is known as n-type semiconductor. As the pentavalent atom is dopped, four out of five valence electrons form four covalent bond with the nearby four other atoms of the crystal. During this the fifth electron remains unbounded. This electron moves randomly in crystal and increases the conductivity of crystal. Therefore, it is called n-type or donor type semiconductor.

Thus the free electrons are the charge carriers in n-type semiconductor which makes them almost independent of increase in temperature. However, the increase in temperature creates thermally generated holes and free-electrons pairs. So, the free electrons are the majority charge carriers and holes are minority charge carriers.

Despite of pentavalent atoms being dopped to form n-type semiconductor, it is electrically neutral. It is so because the pentavalent atoms which are dopped are electrically neutral and pure semiconductor too.

b) <u>P-type semiconductor or acceptor type</u>:

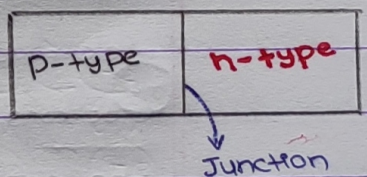


When trivalent impurity or atoms like indium (In) are added or dopped to pure Ge or Si crystal, then the resulting crystal is known as p-type semiconductor. As the trivalent atom is dopped, these valence electrons of the dopped atom forms three complete covalent bond with the nearby three other atoms of the crystal. And an incomplete covalent bond having the presence of hole is formed. This hole at once captures the electron of the neighbouring covalent bond and a new hole is formed at that bond and so on. Thus the positive hole moves randomly inside the crystal and increases the conductivity of crystal. This makes the p-type semiconductors almost independent of increase in temp. However, the increase in temp. creates thermally generated holes. So, the holes are majority charge carriers and free electrons are minority charge carriers.

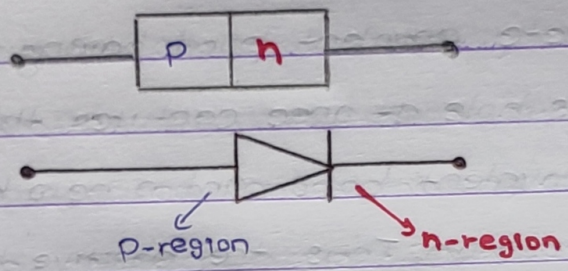
Despite of trivalent atoms being dopped to form p-type semiconductor, it is electrically neutral. It is so because the trivalent atoms which are dopped are electrically neutral and semiconductors too.

p-n junction diode or Junction diode or semiconductor diode:

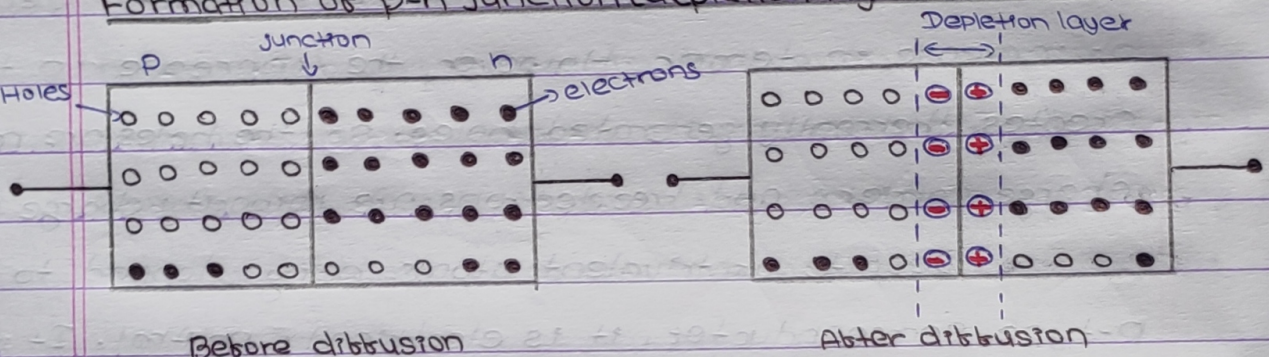
→ When p-type and n-type semiconductors are joined together at a junction, then p-n junction is formed. However it is not formed by joining p-type semiconductor with n-type in real practice.



It is formed by dopping certain no. of pentavalent atoms in one end of the pure semiconductor with equal no. of trivalent atoms on the other end of the same conductor. The circuit symbol of p-n junction diode is as shown below:



Formation of p-n junction (depletion layer & barrier potential)



As soon as the p-n junction diode is formed there occurs the difference in the concentration of charge carriers. The p-region has majority of holes and minority of free electrons whereas the n-region has majority of free electrons and minority of holes. Due to the difference in the concentration of charge carriers there occurs the diffusion of hole from p-region to n-region and free electrons from n-region to p-region. During the process

the free electrons and holes are recombined near the junction. Due to the recombination, the region near the junction is depleted (emptied) of free electrons and holes which is known as depletion layer or depletion region. Its width is about 10^{-3} cm to 10^{-6} cm.

And during the process of diffusion, +ve ion is created besides the junction in n-region and -ve ion is created besides the junction in p-region. After sometime a wall of positive ion and negative ion is created besides the junction which further prevents the diffusion of charge carriers. Thus, a potential difference called Barrier potential is set up across the junction. Its value depends on the nature of crystal, its temp^{re} and the amount of dopping. The value of barrier potential is about 0.3V for Ge and 0.7 V for Si at room temp^{re}.

Biasing of p-n Junction:

The process of connecting the p-n junction diode to an external source or battery for its operation is known as biasing of diode. A p-n junction can be baised in two ways:

1) Forward biasing:

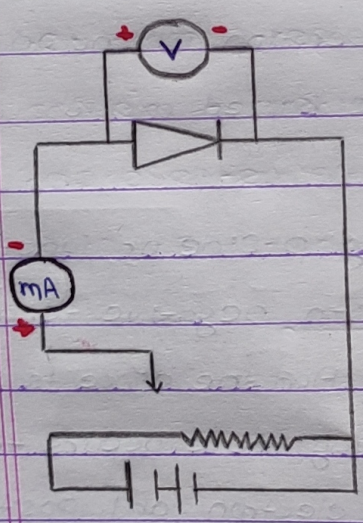
→ The process of connecting p-side of junction with positive terminal and n-side with negative terminal of a battery is called forward biasing. And the diode is said to be forward biased. In forward biasing there occurs the repulsion betwn negative terminal and free electron and positive terminal

towards the junction. The width of depletion layer is reduced and the value of barrier potential is reduced. The junction offers low resistance. The graph between p.d and current is non-ohmic.

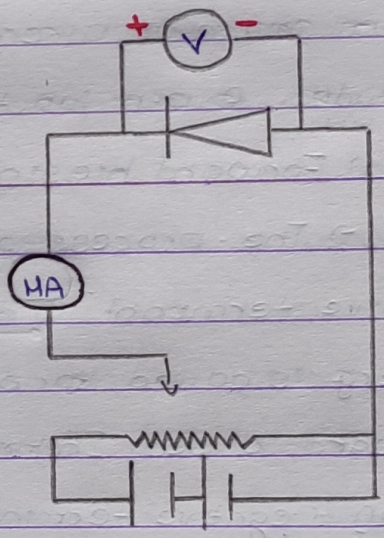
(ii) Reverse biasing:

→ The process of connecting p-side of junction with negative terminal and n-side with positive terminal of battery is called reverse biasing. And the diode is said to be reverse biased. In reverse biasing, there occurs the attraction between holes and negative terminal and free electrons and positive terminal away from the junction. The width of depletion layer is increased and value of barrier potential is increased. The junction offers high resistance. And the graph between pd and current is also non-ohmic.

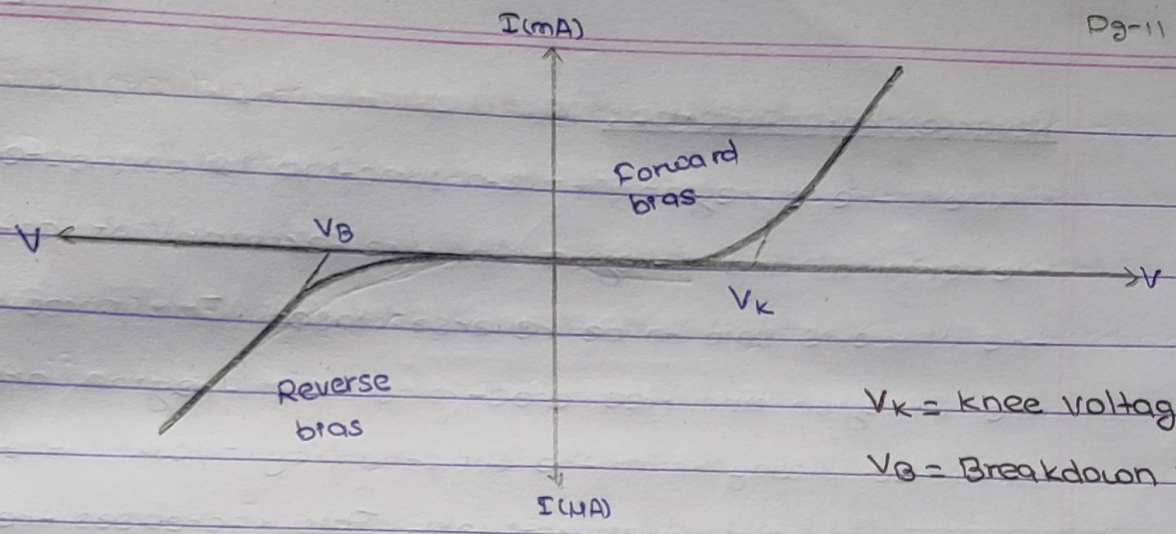
Characteristics of p-n junction:



Forward biasing of diode



Reverse biasing of diode



V_k = knee voltage

V_B = Breakdown voltage

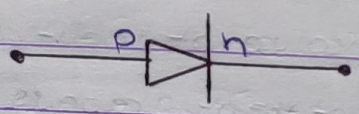
Forward characteristics:

When p-region of p-n junction is connected to 'tve' terminal and n-region is connected to '-ve' terminal of battery the diode is said to be forward biased. The holes in the p-region and free electrons in n-region are repealed towards the junction by the tve and -ve terminal of battery. During this process the value of potential is plotted along x-axis and current along y-axis. The current does not flow through the diode initially even for the increase in potential. But as the value of potential reaches close to the knee voltage, current just begins to flow. Beyond the value of knee voltage, the current increases largely even for a small change in value of input potential. The reciprocal of slope of graph gives the value of input resistance which is very low. And the nature of graph is as shown in above figure.

Reverse characterristics:

When the p-region of p-n junction is connected to -ve terminal and n-region to -ve terminal of battery the diode is said to be reverse biased. The holes in the p-region and free electrons in n-region are attracted away from the junction by -ve and +ve terminal of battery respectively. This increases the width of depletion layer. So, almost no current passes through the diode. However, a small current of few microampere still passes due to minority charge carries free electron in p-region and holes in n-region. The battery connection which does not permit current through the p-n junction is called reverse bias. At high reverse bias breakdown voltage (V_B), the junction breaks and current increases rapidly as shown in the graph above.

As p-n junction permits unidirectional current i.e. from p-region to n-region only when it is forward biased, therefore it is called diode and is represented as

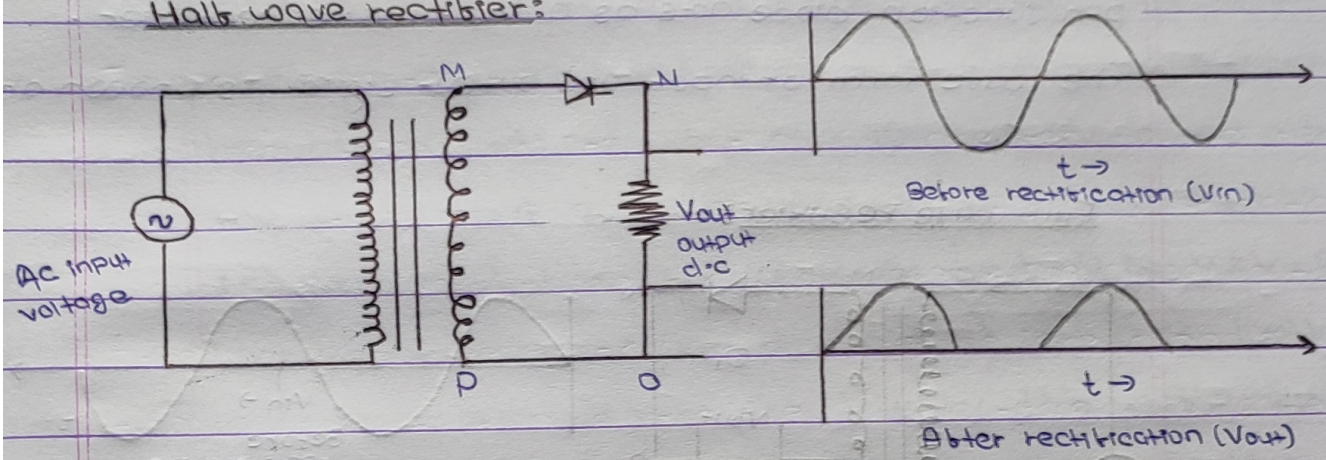


Semiconductor diode as a rectifier:

The process of converting A.C into d.c. is called rectification and the device which converts a.c to d.c is called rectifier. A semiconductor diode acts as a rectifier. There are two types of rectifier:

i) Half wave rectifier ii) Full wave rectifier

Half wave rectifier:



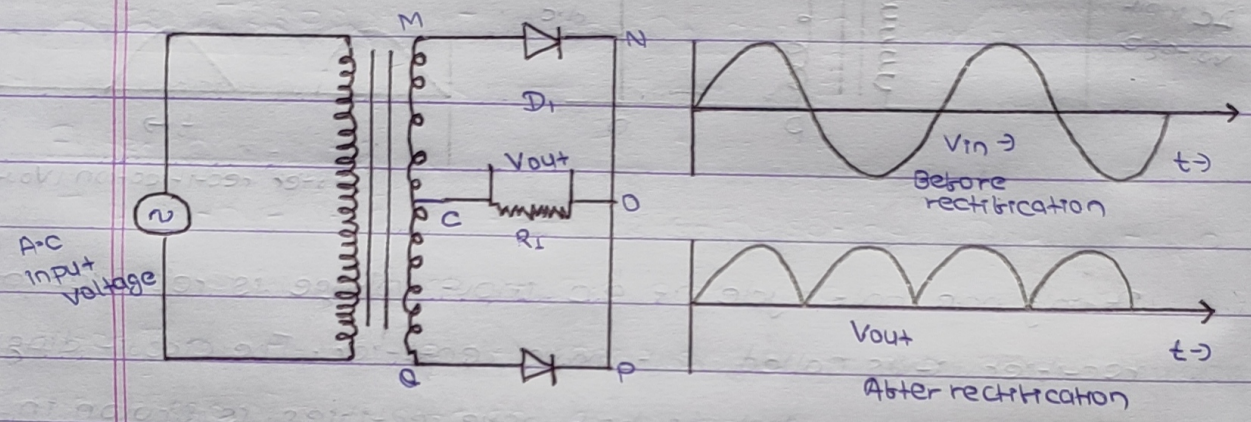
If only one half cycle of a.c input voltage is rectified by the rectifier, it is called half wave rectifier. The circuit diagram of p-n junction diode as half wave rectifies is shown in figure above. It consists of a step down transformer and p-n junction diode as connected above.

During the 1st +ve half cycle of the a.c input voltage, let the potential at end M is $V = V_0 \sin(\omega t + \phi)$ and the potential at point P on next end is O. Due to the difference in potential current tends to flow along the path MNOPM. As the diode is forward biased during the same output is

obtained across the load resister R_L.

Again, during the 1st -ve half cycle of the a.c input voltage, the potential at end M becomes '0' and the potential at end p becomes $V = V_0 \sin(\omega t + \phi)$. Due to the difference in potential current tends to flow but the diode becomes reverse biased. So, the output is not obtained across the load resister (R_L). Thus a single p-n junction diode acts as a half wave rectifier. The wave form of input and output signal is shown above.

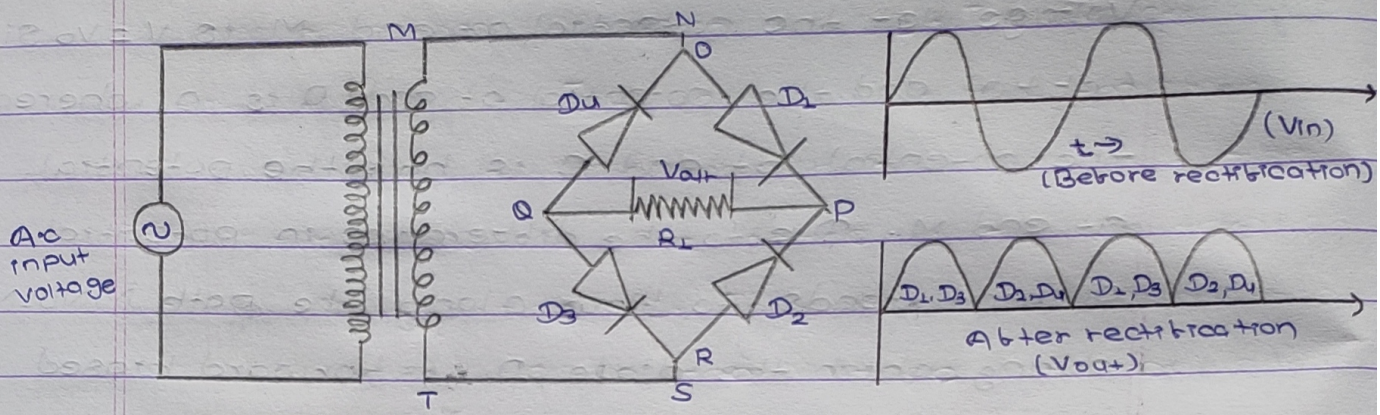
Full wave rectifier:



If both positive and negative half cycle of the a.c and rectified by a rectifier, it is called full wave rectifier. The circuit diagram of two p-n junction diode as full wave rectifier is shown in the figure above. It consists of a centre tapped step down transformer and two p-n junction diode as connected above.

During the 1st +ve half cycle of the ac input voltage let the potential at end M is $V = V_0 \sin(\omega t + \phi)$ and the potential at end Q is 0 whereas the potential at end C is half the potential at end M. Due to the difference in potential, current tends to flow along the path MNQCM during which the diode D_1 is forward biased and the output is obtained across the load resistor. But at that time the diode is reverse biased. Again, during the 1st -ve half cycle of the a.c input voltage, the potential at end M is zero and the potential at end Q is $V = V_0 \sin(\omega t + \phi)$ whereas the potential at end C is half the potential at end Q. Due to the difference in potential current tends to flow along the path QPOCQ during which the diode D_2 is forward biased and output is obtained across the load resistor. But at the same time diode D_1 is forward biased. The output is continued for all the other a.c input voltage. The waveform of input and output signal is as shown above.

(ii) Bridge rectifier:



* During first +ve a.c input cycle; current flows along MNOPQRSTM and D_1 and D_3 are forward biased.
* During first -ve a.c input cycle; current flows along TSRPQONMT and D_2 and D_4 are forward biased

Filter circuit:

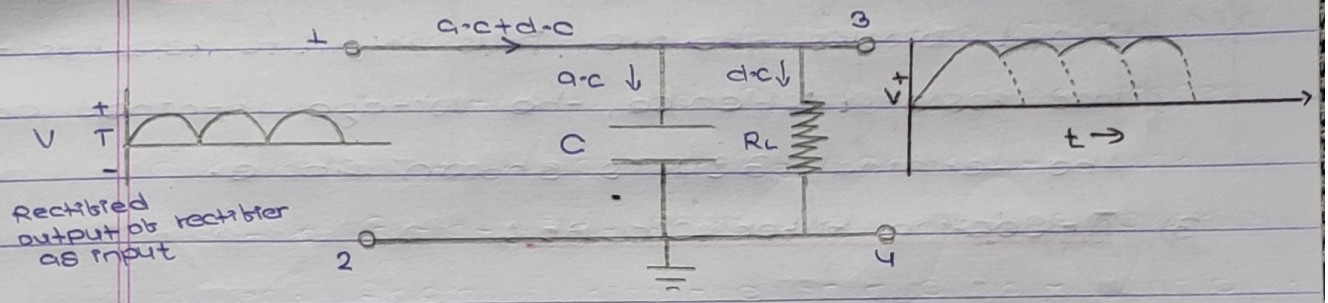
The output of a voltage is a pulsating D.c voltage which is a mixture of a.c and d.c voltage. So, a filter circuit is used to remove a.c voltage and provide d.c voltage only. Electrical components like capacitor and inductor are used widely for making filter circuits. The different types of filter circuits are:

i) Shunt capacitor filter
ii) Inductor filter
iii) Choke or L.C filter
iv) π filter

Note:

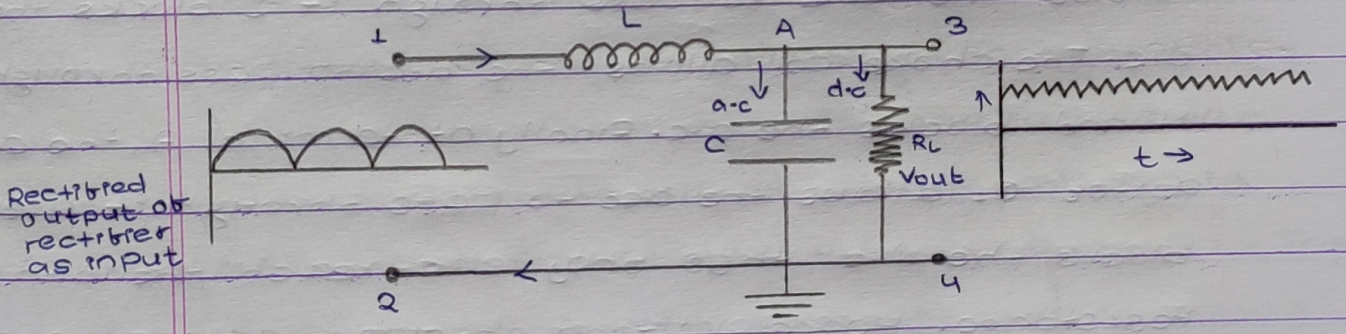
	A·C	D·C
Inductor - $X_L = \omega L = 2\pi fL$	Blocks the flow	Allows the flow (series)
Capacitor - $X_C = 1/\omega C = 1/2\pi fC$	Allows the flow	Blocks the flow (Parallel)

1) Shunt capacitor filter circuit:



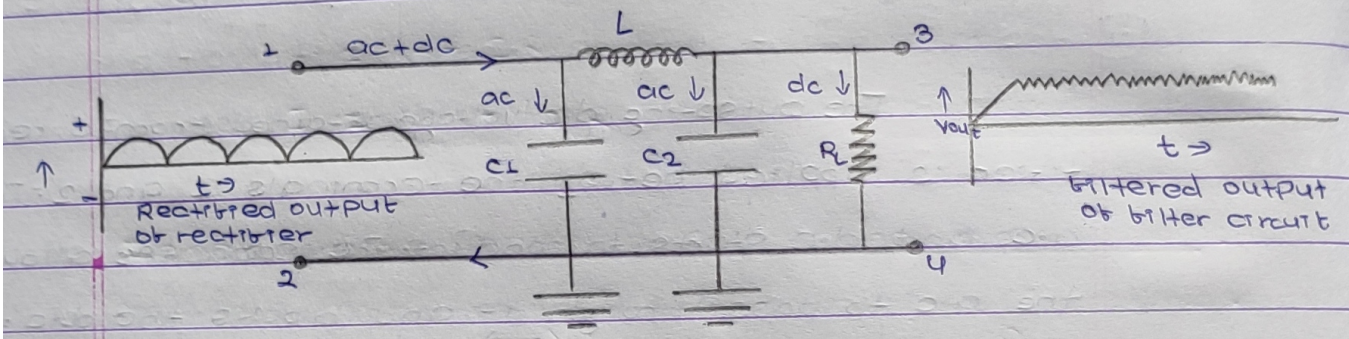
The pulsating d·c voltage obtained from a rectifier is applied between the terminals 1 and 2. The a·c and d·c starts to conduct. The capacitor allows the a·c to pass through it and blocks the d·c. Thus only d·c reaches the load resistance. Hence, the voltage obtained across the terminal 3 & 4 is shown above.

2) Choke input filter circuit



The pulsating d.c voltage obtained from a rectifier is applied between the terminal 1 & 2. The a.c and d.c starts to conduct. The choke coil blocks the a.c and allows the d.c to pass through it. Again at 'A' the capacitor allows the rest of the a.c to pass through it and blocks the d.c. Thus, only d.c reaches the load resistor. Hence, the voltage obtained across the terminal 3 & 4 is shown above.

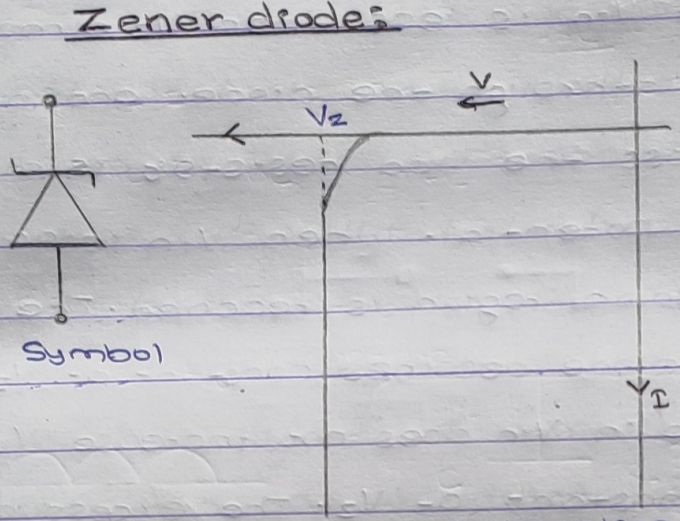
3) π - Section filter circuit :



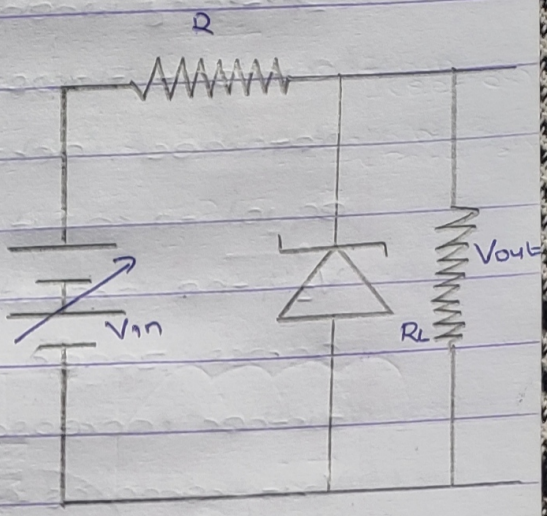
The pulsating d.c voltage obtained from a rectifier is applied between the terminal 1 and 2. The a.c and d.c starts to conduct. The capacitor C_1 allows the a.c to pass through it & blocks the d.c. The choke coil allows the d.c to pass through it and blocks the a.c. Finally at terminal A, the capacitor C_1 allows the a.c to pass through it and blocks the d.c, thus only d.c reach the load resistance. Hence, voltage obtained across terminal 3 and 4 is as shown in graph which is max d.c voltag

V.V.Imp

Zener diode:



V-I characteristics in reverse bias connection



Circuit as voltage stabilizer

A specially designed p-n junction diode to work in reverse bias voltage is called zener diode. The symbol and V-I characteristics in reverse bias of zener diode is shown in figure above. It has a sharp breakdown voltage called zener voltage (V_z). The voltage across zener diode is constant at zener voltage whatever be the large current through it. Thus, zener diode can be used as voltage stabilizer.

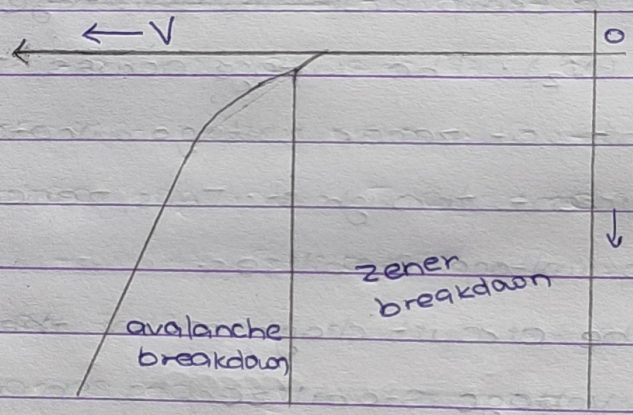
The circuit diagram for the zener diode as a voltage stabilizer is shown in figure. The different input voltage is applied at Vin however the stabilized output voltage is is obtained across the load resistor R_L. The graph betwn V_o and V_I is shown in figure.

Initially when V_{in} is less then V_z almost no current flows through the diode. and output obtained across the load resistor is almost equal to input potential. When V_{in} is equal to V_z, the breakdown region is reached. The voltage across zener diode becomes constant at V_z. Any further increase in V_{in} does not increase V_{out} but V_{out} remains constant at V_z. The excess of V_{in} appears across the limiting resistance R. In that case, we have

$$V_{in} = V_z + IR$$

$$\text{or, } I = V_{in} - V_z/R$$

Zener breakdown and avalanche breakdown:



If p-type and n-type in a p-n junction diode is heavily dopped then the depletion layer is thin. The small reverse biased battery voltage is eno-

ugh to break the junction bor the rapid increase ob current. This type ob breakdown is called zener breakdown and takes place in zener diode.

Ib p-type and n-type ob a p-n junction diode are lightly dopped then the depletion layer is wide. The minority carriers electrons in p-type are repealed by negative reverse biased battery voltage. These electrons collide with the atoms. The covalent bonds ob the atoms break. The new electrons are liberated. These electron burther collide with another atom and so on. Thus, avalanche ob electron are liberated, the current increases gradually. This type ob breakdown is called avalanche breakdown and takes place in ordinary diode.

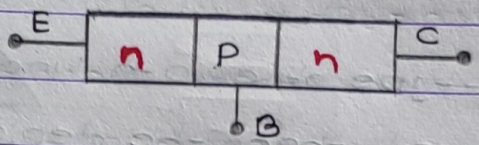
Transistor

Transistor is composed ob two words, transber and resistor. Thus, it is debined as the resistor which amplibies the input signals brom input to output. A transistor is bormed by joining two semi-conductors diodes together.

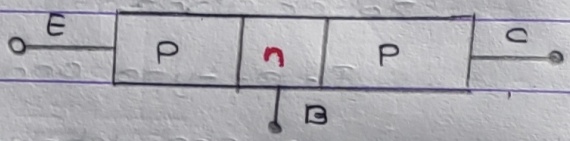
It is of two types:

i) NPN / npn transistors

ii) PNP / pnp transistor

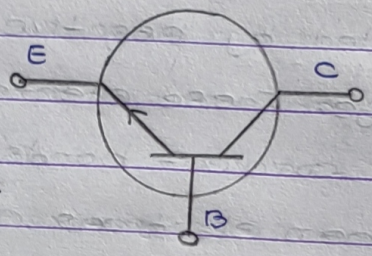


Block diagram

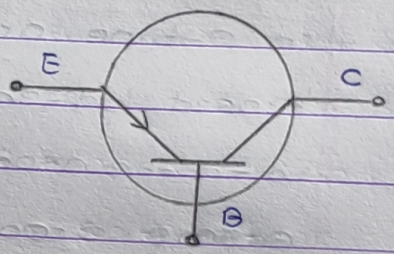


Block diagram

E → emitter
B → Base
C → collector



Symbol of npn transistor



Symbol of pnp transistor

If p-sides of two diodes are joined together then npn transistor is formed.

If n-sides of two diodes are joined together then pnp transistor is formed. Both the transistors have three regions. They are

i) Emitter (E) ii) Base (B) iii) Collector (C)

i) Emitter (E):

→ Emitter is heavily dopped region and it supplies charge carriers to the base region and finally to the collector. It has larger region than base and smaller than the collector.

ii) Base(B):

→ Base is a lightly dopped region and very thin in order of 10^{-6} m. It has smallest region.

iii) Collector(C):

→ The collector is dopped so that its dopping level lies betwn that of emitter and base. It collects the charge carriers from the base and hence the name collector. It has the largest region in the transistor.

→ Biasing of transistor:

The process of connecting the transistor to an external source or battery is known as biasing of transistor. As the transistor has only three terminal one of three terminals is made common to both input and output section. The rules of biasing are as follows:

i) The emitter and base of the transistor is always forward biased for normal operation.

ii) The collector and base of the transistor is always reverse biased. In other words, the polarity of collector and base is always same with respect to the polarity of emitter.

The different types of transistor biasing are as follows:

1) Forward active mode:

→ When the emitter-base junction is forward biased and the collector-base junction is reverse biased, the transistor is said to be in forward active mode. In this mode, a large amount of collector current is obtained.

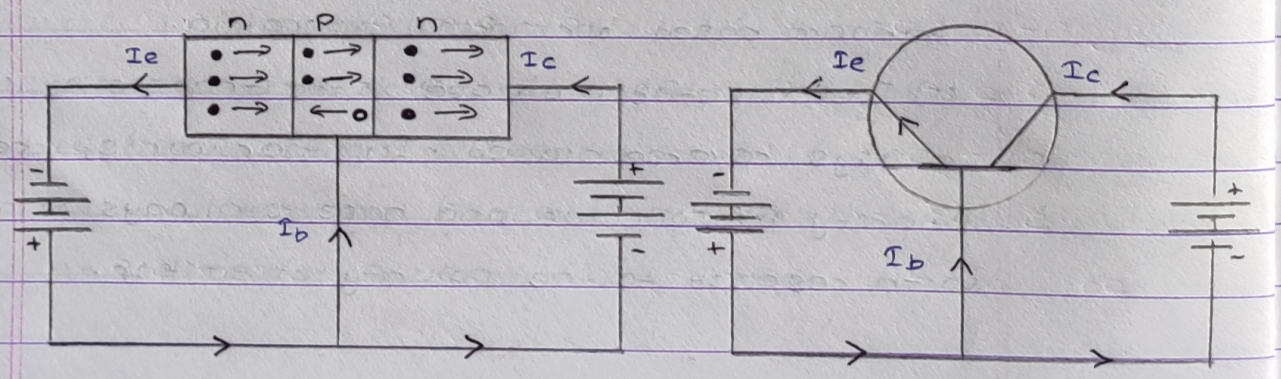
2) Saturation mode:

→ When both the emitter and base as well as base and collector are forward biased, the transistor is said to be in saturation mode. In this mode, the transistor acts as closed switch

3) Cut-off mode:

→ When both the emitter and base as well as base and collector are forward biased, the transistor is said to be in cut-off mode. In this mode transistor acts as a open switch.

Working of n-pn transistor:



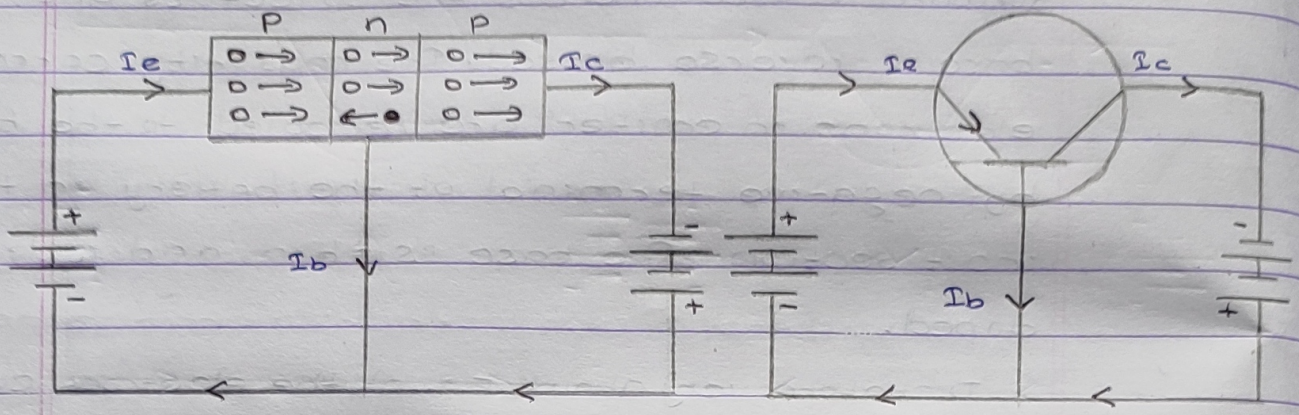
The emitter and the base of the transistors is forward biased whereas the collectors and base is reverse biased. The majority carrier electrons in emitter are repealed to the base by negative terminal of the battery in the input section. The base is thin and is lightly doped.

Therefore very about 5% of the electrons coming from the emitter are combined with holes in the base region. The rest of the electrons reaches the collector region where they are attracted by positive terminal of battery in the output section. The electrons reaches to the emitter continuously from the -ve terminal of battery in the input section and the same number of electrons are attracted by the positive terminal of the battery in output section. Thus, current passes through the circuit in the opposite to the flow of electron.

If I_e, I_b and I_c are the emitter, base and collector current then

$I_e = I_b + I_c$ [using Kirchoff's law of current]

Working of pnp transistores:



The emitter and base of the transistor is forward biased and the collector and base is reverse biased. The majority charge carriers are holes in the emitter which are repealed by positive terminal of the battery in the input section towards the base. The base is lightly dopped and thin. Therefore, very few about 5% of holes coming from emitter are combined with electrons in the base region. The rest of holes reaches the collector region where they are attracted by the -ve terminal of the battery in the output section. The holes in the collector region attract the electrons from the -ve terminal of the battery. In the output section same numbers of electrons leaves the emitter as they are attracted by the positive terminal of the battery.

The current passes continuously through the circuit in the direction of the flow of the holes.

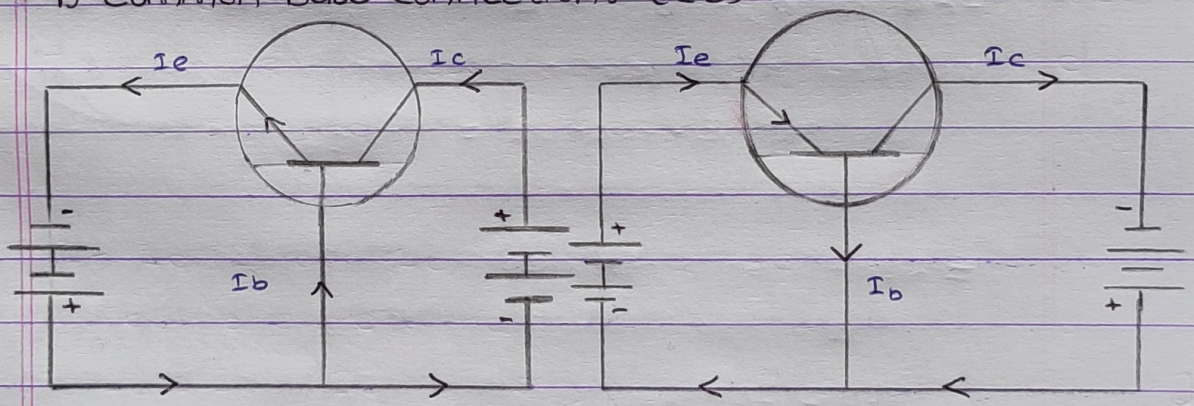
If Ie, Ib and Ic are the emitter, base and collector current then,

$I_e = I_b + I_c$ [using kirchoff's law of current]

Configurations of transistors:

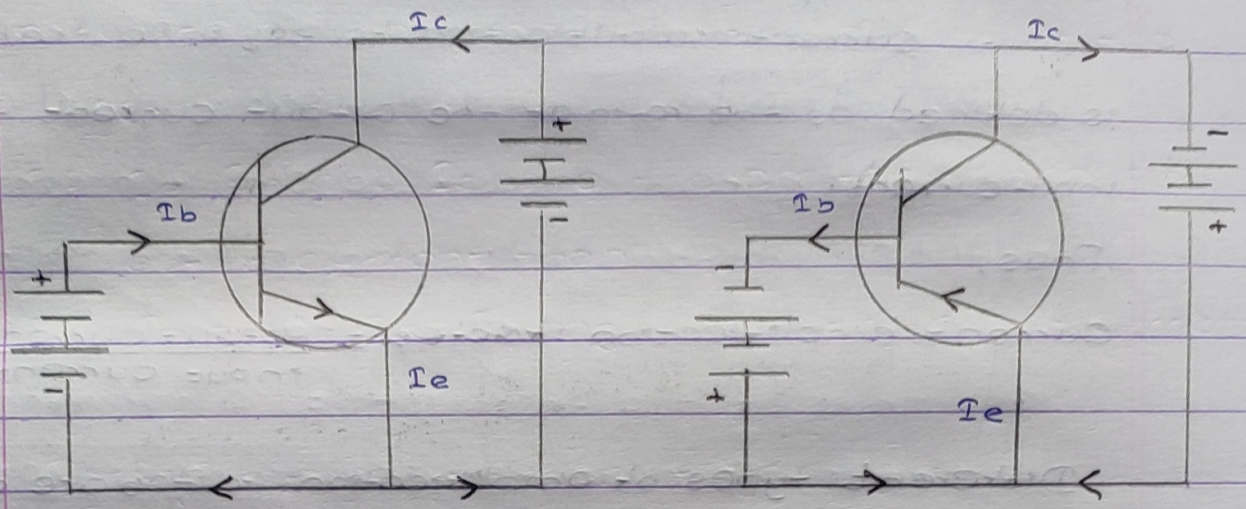
A transistor has three terminals & four terminals are required when it is connected in circuit. Two of terminals for input and two for the output. This is done by using one of the three terminals as common terminal to the input and output section. Thus, there are three ways of configuration of transistor.

1) Common base connection: (CB)



Ie = input current
Ic = output current

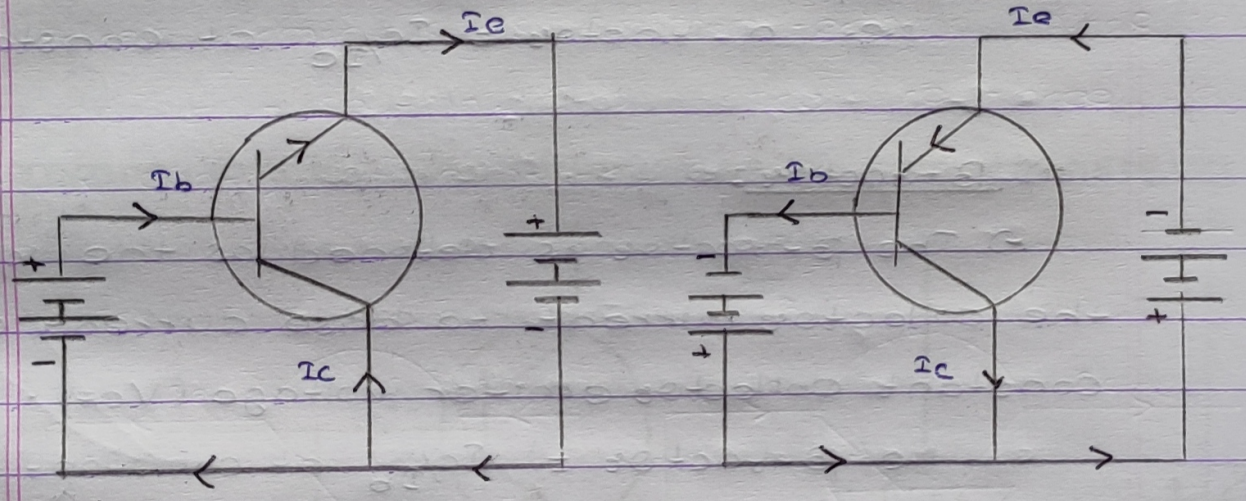
(ii) Common emitter configuration (CE)



I_b = input current

I_c = output current

(iii) Common collector configuration (CC)



I_b = input current

I_e = output current

Current amplification factor

→ Current amplification factor in a transistor is defined as the ratio of the output current to input current.

Thus,

current amplification factor = $\frac{\text{output current}}{\text{input current}}$

Different types of amplification factor are as follows:

i) **α - factor:**

→ The α-factor is defined as the ratio of the collector current to the emitter at constant collector base voltage (V_{CB}).

i.e. α - factor = I_c/I_e at constant V_{CB}

ii) **β - factor:**

→ The β-factor is defined as the ratio of the collector current to base current at constant collector emitter voltage (V_{CE}).

i.e. β - factor = I_c/I_b at constant V_{CE}

Relationship between α and β:

We know that,

$I_e = I_c + I_b$

Dividing both sides by I_c,

$I_e/I_c = 1 + I_b/I_c$

$$\text{or, } \frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\text{or } \frac{1}{\alpha} = \frac{\beta+1}{\beta}$$

$$\text{or, } \alpha = \frac{\beta}{\beta+1} \quad \text{i.e. } \alpha \text{ is always less than 1.}$$

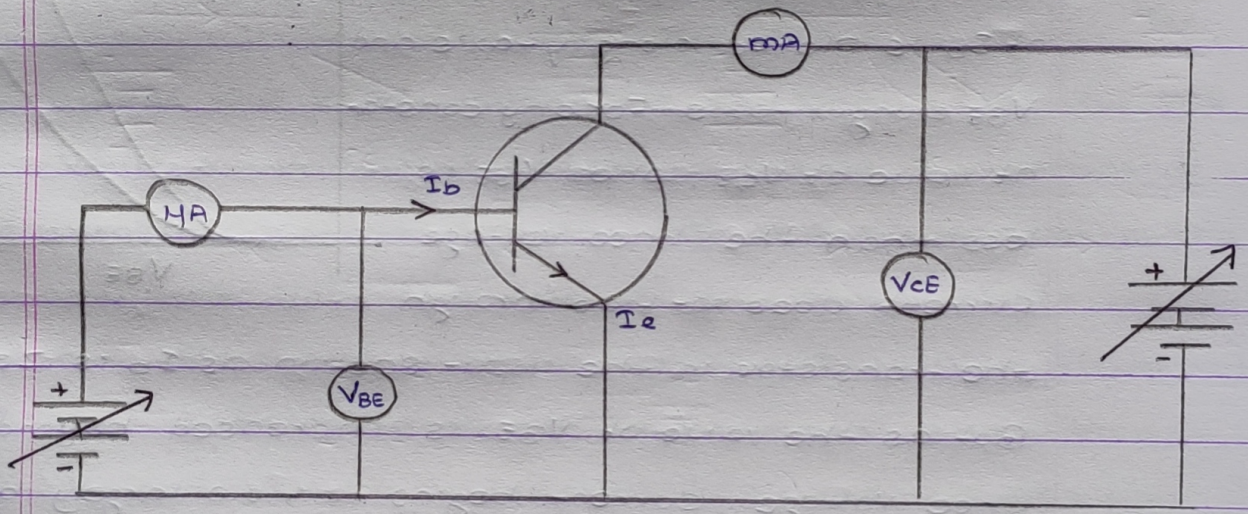
Also,

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\text{or, } \frac{1}{\beta} = \frac{1}{\alpha} - 1 = \frac{1-\alpha}{\alpha}$$

$$\text{or } \beta = \frac{\alpha}{1-\alpha} \quad \text{i.e. } \beta \text{ is always more than 1.}$$

Common emitter characteristics of npn transistor:

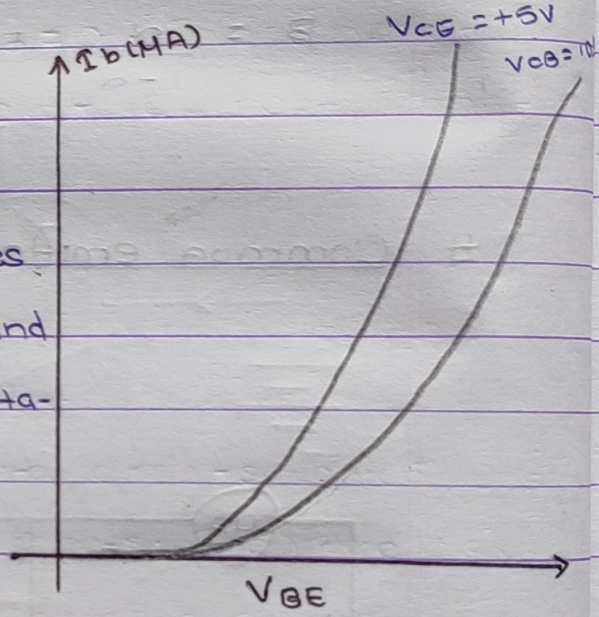


Circuit diagram of npn transistor in CE configuration

In a common emitter connection, the relation between the current and the voltage can be represented graphically which is known as common emitter characteristics. The circuit diagram of the common emitter configuration of npn transistor is as shown in the figure above. The emitter and base of the transistor is forward biased whereas the collector and base is reverse biased making emitter common to both input and output section. The different characteristics of npn transistor in CE configuration are as follows:

1) Input characteristics:

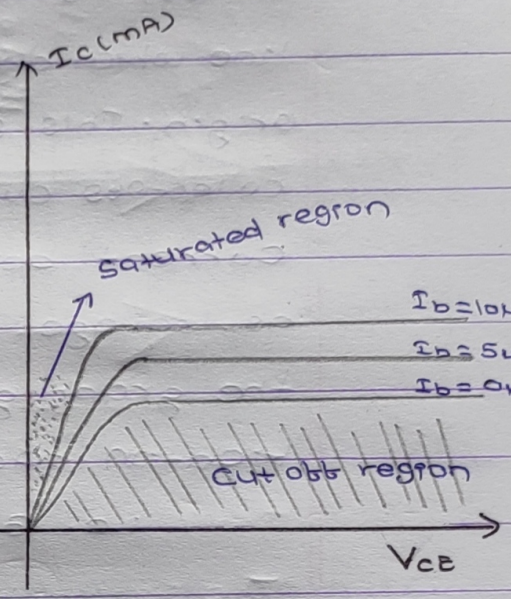
⇒ It is the graph between V_{BE} & I_b at constant V_{CE}. The values of I_b is plotted along y-axis and V_{BE} along x-axis. For any constant value of V_{CE}, when V_{BE} is less than the knee voltage current does not flow through the transistor in the input section as I_b is zero. But as the value of V_{BE} is increased beyond the knee voltage, current begins to flow largely between base and emitters for even small change in V_{BE}. The nature of graph obtained is as shown above.



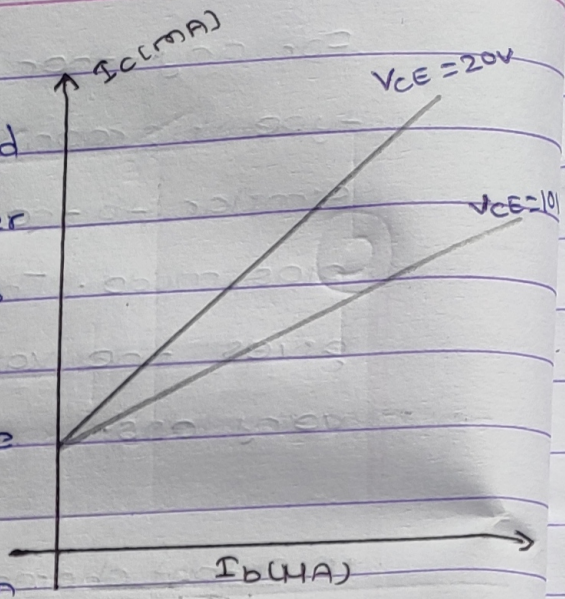
For any other constant value of V_{CE}, similar type of graph is obtained. The graph obtained is similar to the graph of pn junction in forward bias mode. The reciprocal of the slope of graph gives the value of input resistance which is very less.

ii) Output characteristics:

→ It is the graph between V_{CE} and I_C at constant I_b. The value of I_e is plotted along y-axis and V_{CE} along x-axis. For any constant value of I_b the value of I_C increases rapidly even for very small change in V_{CE}. This occurs unless the knee voltage is obtained. Beyond the value of knee voltage the value of I_C remains almost constant despite for the increase in the value of V_{CE}. The nature of the graph is as shown in the above figure. It is also observed that the value of I_e is not zero even for $I_b = 0\mu A$, this current is known as leakage current. The reciprocal of the slope of graph gives the value of output resistance which is very large.



iii) Transfer characteristics:



→ It is the graph between Ic and Ib for constant collector emitter voltage (V_{CE}). The value of Ic is plotted along y-axis and Ib is along x-axis. For constant value of V_{CE}, we obtain a straight line which does not pass through origin. This shows that the collectors current is not zero even for base current being zero. This current is known as leakage current for $I_b = 0$. The slope of the graph gives the value of current amplification factor β.

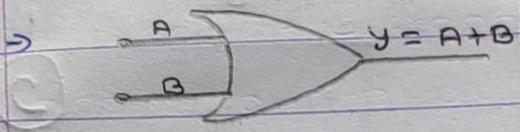
i.e. $$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Logic gates

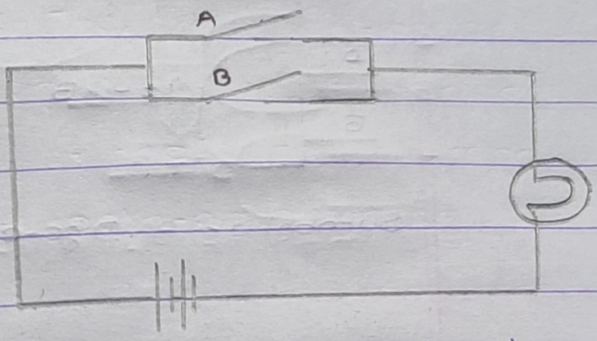
Logic gates are the digital circuits which gives logical decisions for the given inputs. They are also circuits in which transistor act as a high speed switches. They are the basic building blocks of every digital circuits. The Boolean equation relates the input and output in digital circuit. The result of output signals of a logic circuit can be predicated for the given input signals in a form of a table called as truth table.

Different types of logic gates are as follows:

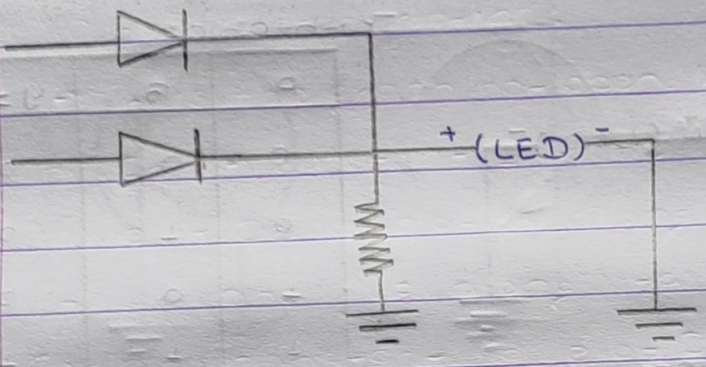
1) OR gate:



Symbol of OR gate



Circuit realization of OR gate



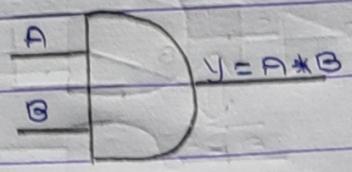
Circuit diagram of OR gate

Truth table

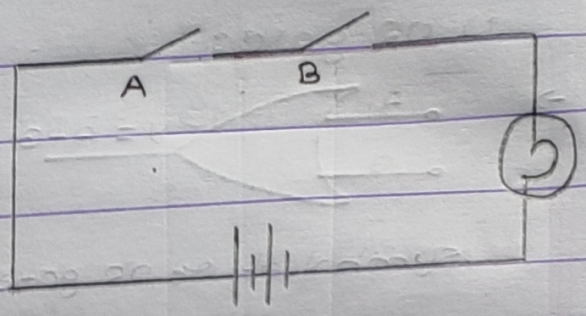
A	B	y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

The symbol and circuit diagram of OR gate is as shown in figure above. It consists of two or more than two inputs and only one output. The Boolean equation of two input OR gate is given as $y = A+B$, where y is the output and, A & B are inputs. It is one sensitive gate and gives high output when at least one or the two input is high. The truth table of OR gate is shown above.

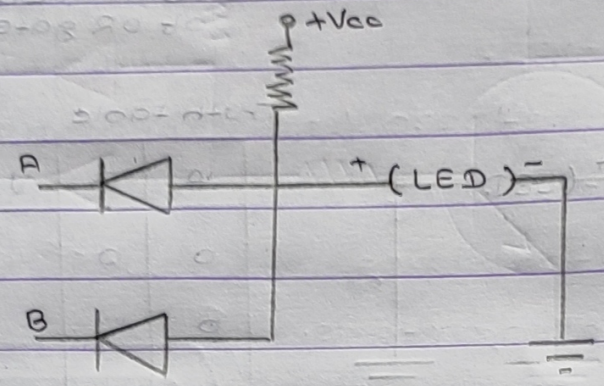
ii) AND gate



Symbol of AND gate



Circuit realization of AND gate



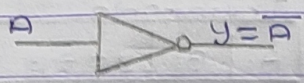
Circuit diagram of AND gate

Truth table:

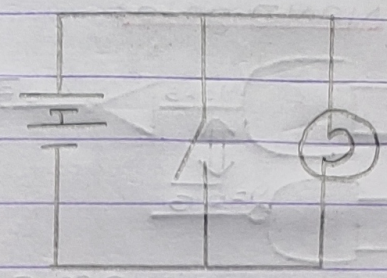
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

The symbol and circuit diagram of AND gate is as shown in figure above. It consists of two or more than two inputs and only one output. The Boolean equation of two input AND gate is given as $y = AB$ where y is the output and A & B are the inputs. It is zero sensitive gate and gives low output when at least one of the input is low. The truth table and gate is shown above.

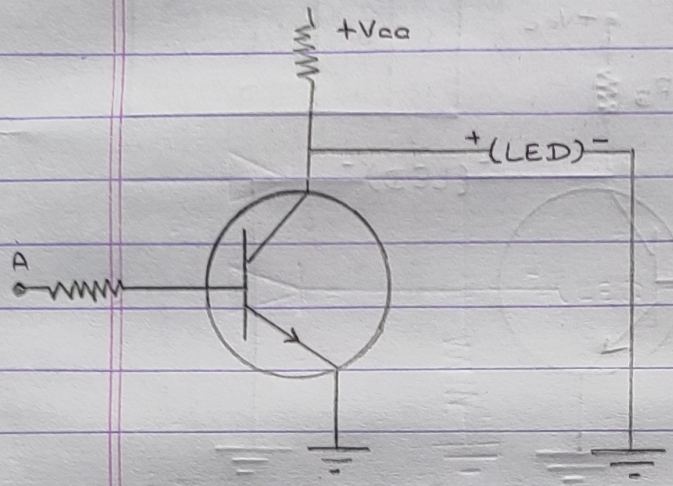
iii) NOT gate



Symbol of NOT gate



circuit realization of NOT gate



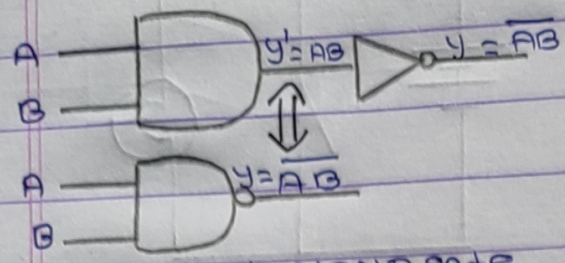
Circuit diagram of NOT gate

Truth table:

A	y = Ā
1	0
0	1

The symbol and circuit diagram of NOT gate is as shown in figure above. It consists of one input and only one output. The Boolean equation of NOT gate is $y = \bar{A}$ where, A is input and y is output. It is also known as inverter and gives inverted output. The truth table of NOT gate is as shown above.

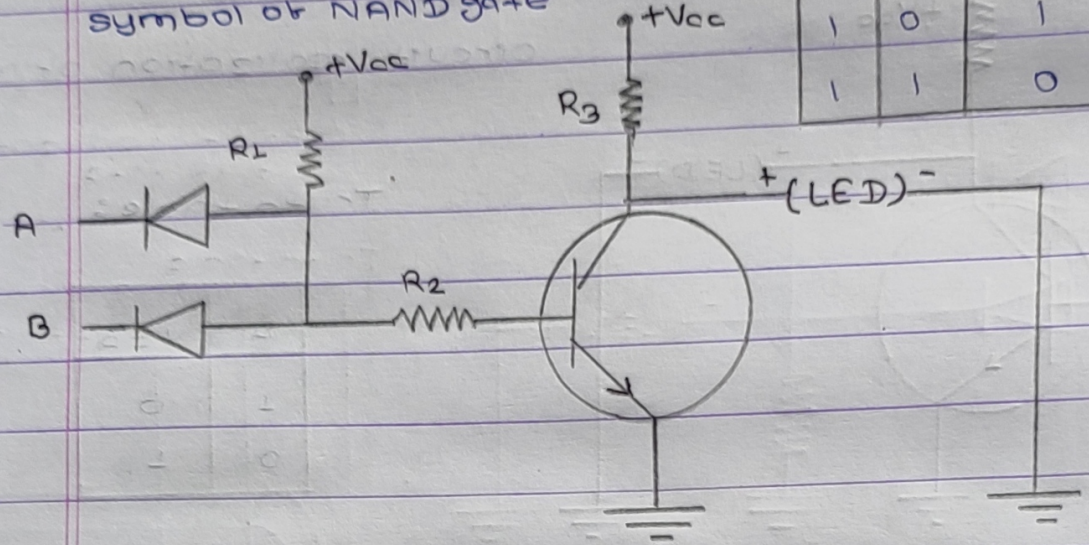
(V) NAND gate:



Symbol of NAND gate

Truth table

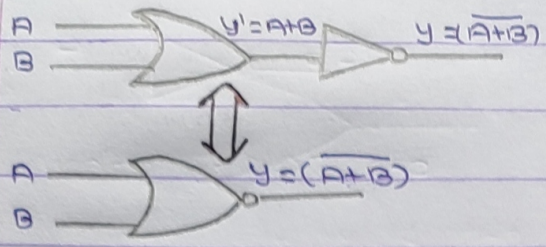
A	B	y = $\overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0



Circuit diagram of NAND gate

The symbol and circuit diagram of NAND gate is as shown in figure above. It consists of two or more than two inputs and only one output. The Boolean equation of two input NAND gate relating input and output is $y = \overline{AB}$ where A & B are inputs and y is output. It gives the inverted output of AND gate and gives low out put when both inputs are high. The truth table of NAND gate is shown above.

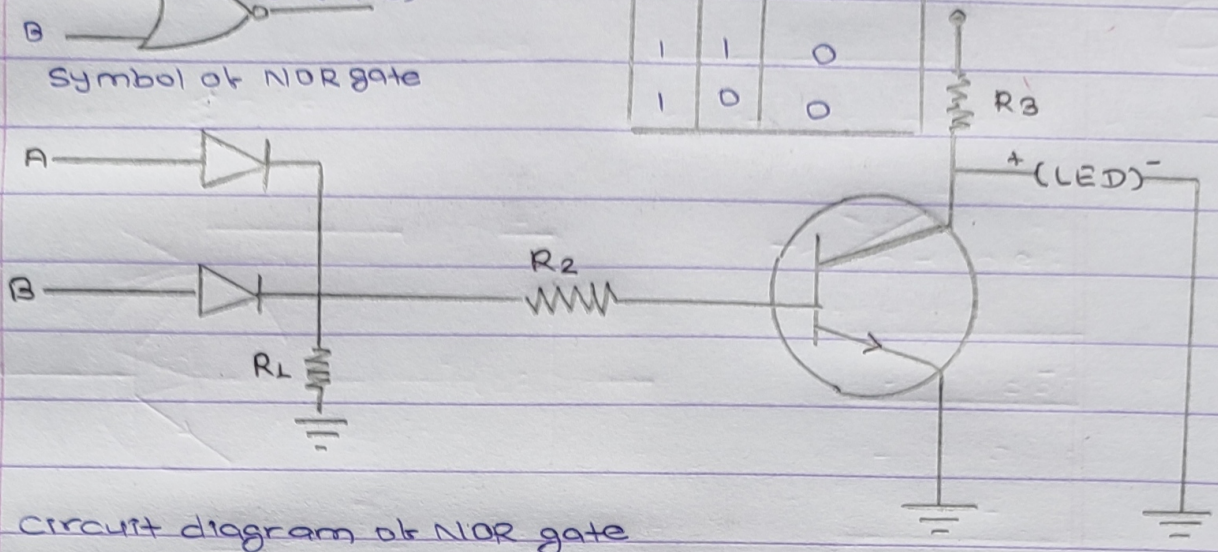
v) NOR gate:



Symbol of NOR gate

Truth table:

A	B	y = $\overline{A+B}$
0	1	1
0	0	0
1	1	0
1	0	0



Circuit diagram of NOR gate

The symbol and circuit diagram of NOR gate is as shown above. It consists of two or more than two inputs and only one output. The Boolean equation of two input NOR gate is given as $y = \overline{A+B}$. where y is the output and A & B are the inputs. It gives the inverted output of OR gate and gives high output when both inputs are low. The truth table of NOR gate is shown above.

prepare a short note on "Nanotechnology".